

## IN THE ABSTRACT

Please replace the Abstract with the Abstract attached herewith.

## IN THE CLAIMS

Please amend claims 1-2, 4-11, and 13-14 as follows. All claims have been provided as a courtesy to the Examiner.

1 1. (Twice Amended) A memory module controller for providing an interface  
2 between a system memory controller and a plurality of memory devices on a memory  
3 module, comprising:  
4 first interface circuitry [configured] to receive from the system memory  
5 controller a first memory transaction in a first format; and  
6 control logic coupled to the first interface circuitry and [configured] to convert the  
7 first memory transaction into a second memory transaction in a second format for the  
8 plurality of memory devices, wherein the second format of the second memory transaction  
9 is different from the first format of the first memory transaction.

1 2. (Twice Amended) The memory module controller of claim 1, further  
2 comprising:  
3 second interface circuitry coupled to the control logic and [configured] to transmit  
4 the second memory transaction to at least one of the plurality of memory devices.

1 3. (Unchanged) The memory module controller of claim 1, wherein the first memory  
2 transaction includes time multiplexed address and command information.

1 4. (Twice Amended) The memory module controller of claim 3, wherein the first  
2 interface circuitry comprises:  
3 request handling logic [configured] to separate the address and command  
4 information and to provide the separate address and command information to the control  
5 logic.

1 5. (Twice Amended) The memory module controller of claim 4, wherein the first  
2 memory transaction further includes time multiplexed data information, and wherein the  
3 request handling logic is [further configured] to separate the time multiplexed data  
4 information and to provide the separated time multiplexed data information to the control  
5 logic.

1 6. (Twice Amended) The memory module controller of claim 1, wherein the first  
2 interface circuitry comprises:  
3 handshaking logic [configured] to provide a handshake signal to the system memory  
4 controller that indicates when the memory module controller is communicating data to the  
5 system memory controller.

1 7. (Twice Amended) The memory module controller of claim 1, wherein the first  
2 interface circuitry comprises:  
3 data handling logic [configured] to receive data for the first memory transaction  
4 from the system memory controller and to reformat the data for the second memory  
5 transaction.

1 8. (Twice Amended) The memory module controller of claim 1, further  
2 comprising:  
3 a write buffer coupled to the first interface circuitry and [configured] to store data  
4 sent with the first memory transaction.

1 9. (Twice Amended) The memory module controller of claim 8, further  
2 comprising:  
3 an address storage unit coupled to the write buffer and the first interface circuitry  
4 and the address storage unit is [configured] to store addresses associated with the data  
5 stored in the write buffer.

1 10. (Twice Amended) The memory module controller of claim 1, further  
2 comprising:  
3 a read buffer coupled to the control logic and [configured] to store data read from at  
4 least one of the plurality of memory devices.

1 11. (Twice Amended) The memory module controller of claim 1, further  
2 comprising:  
3 a clock generator circuit coupled to the control logic and [configured] to receive a  
4 first clock signal from the system memory controller and to generate a second clock signal  
5 for the plurality of memory devices.

1 12. (Unchanged) A memory module controller for providing an interface between a  
2 system memory controller and a plurality of memory devices on a memory module,  
3 comprising:  
4 means for receiving from the system memory controller a first memory  
5 transaction in a first format; and  
6 means for converting the first transaction into a second memory transaction in a  
7 second format for the plurality of memory devices, wherein the second format of the second  
8 memory transaction is different from the first format of the first memory transaction.

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1 13. (Twice Amended) A memory module controller for providing an interface  
2 between a system memory controller and a plurality of memory devices on a memory  
3 module comprising:  
4 first interface circuitry [configured] to receive from the system memory  
5 controller a first memory transaction in a first format; and  
6 control logic coupled to the first interface circuitry and [configured] to reformat the  
7 first memory transaction such that the plurality of memory devices perform the reformatted  
8 first memory transaction.

1 14. (Twice Amended) The memory module controller of claim 13, further  
2 comprising:  
3 second interface circuitry coupled to the control logic and [configured] to receive  
4 from one of the plurality of memory devices a second memory transaction in a second

5 format, wherein the control logic [reformats] is to reformat the second memory transaction  
6 such that the system memory controller [performs] is to perform the reformatted second  
7 memory transaction.

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